REMARKS

Claims 42-48 are pending in the application.

Claims 42-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Al-Shareef, U.S. Patent No. 6,111,285, in view of Thakur, U.S. Patent No. 6,255,159. The Examiner is reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Each of these factors must be shown to establish a *prima facie* case of obviousness, the burden of which is on the Patent Office. Claims 42-48 are allowable over Al-Shareef and Thakur for at least the reason that the references, individually or as combined, fail to disclose or suggest each and every limitation in any of those claims.

Independent claim 42 recites a first silicon layer being more heavily doped with conductivity enhancing dopant than a second silicon-containing layer, the second silicon-containing layer defining an exposed inner periphery of a container and the first silicon-containing layer defining an exposed outer periphery of the container. Claim 42 additionally recites converting at least some of each of the first and second silicon-containing layers to hemispherical grain silicon and forming a dielectric material along the exposed inner and exposed outer peripheries of the container construction. As set forth in applicant's previous response, the combination of Al-Shareef and Thakur fails to disclose or suggest the claim 42 recited forming a container construction having an exposed inner periphery defined by a second silicon-containing layer and an exposed outer periphery defined by a first silicon-containing layer which is more heavily doped with conductivity

enhancing dopant than the second silicon-containing layer, and converting at least some of the first and second layers to hemispherical grain silicon. Accordingly, the combination of Thakur and Al-Shareef does not disclose or suggest each and every element of claim 42.

In the present rejection set forth at pages 2-4, the Examiner does not address the claim 42 recited element of forming a dielectric material along exposed inner and exposed outer peripheries of a container construction, the exposed inner periphery being defined by a second silicon-containing layer and the exposed outer periphery of the container being defined by a first silicon-containing layer. Rather, in the Response to Argument section of the Action, the Examiner indicates reliance upon a third reference, DeBoer, U.S. Patent No. 6,451,661, as disclosing an exposed inner periphery defined by a second silicon-containing layer and an exposed outer periphery defined by a first silicon-containing layer which is more heavily doped than the second silicon-containing layer (present action page 5). This feature is clearly not taught or suggested by the art upon which the present rejection is based. Further, since DeBoer and the present application were commonly owned at the time of the invention, DeBoer is not available as a basis for a § 103 rejection. Therefore, DeBoer cannot be relied upon in the manner indicated by the Examiner. Accordingly, a *prima facie* case of obviousness has not been established and independent claim 42 is allowable over the cited combination of Al-Shareef and Thakur.

Dependent claims 43-48 are allowable over the cited combination of Thakur and Al-Shareef for at least the reason that they depend from allowable base claim 42.

For the reasons discussed above, pending claims 42-48 are allowable. Applicant respectfully requests formal allowance of such pending claims in the Examiner's next action.

Respectfully submitted,

Dated: August 27, 2003 By: Jennifer J. Taylor

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Amendments to the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Claims 1-41. (Cancelled)

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42. (Currently amended) A method of forming a capacitor structure, comprising:

forming a container construction comprising a first silicon-containing layer around a second silicon-containing layer; the first silicon-containing layer being more heavily doped with conductivity-enhancing dopant than the second silicon-containing layer; the second silicon-containing layer defining an exposed inner periphery of the container and the first silicon-containing layer defining an exposed outer periphery of the container;

converting at least some of each of the first and second silicon-containing layers to hemispherical grain silicon; the hemispherical grain silicon from the first silicon-containing layer having a smaller average grain size than the hemispherical grain silicon from the second silicon-containing layer;

forming a dielectric material along the exposed inner and exposed outer peripheries of the container construction; and

forming a conductive material over the dielectric material; the container construction, dielectric material and conductive material together defining at least part of the capacitor structure.

43. (Original) The method of claim 42 wherein the converting comprises:

(1) exposing the at least some of each of the first and second silicon-containing layers to silane gas and a temperature of at least about 550°C for a time of less than or equal to about 2 minutes under a vacuum of less than or equal to about 1×10^{-4} Torr to seed the at least some of each of the first and second silicon-containing layers; and

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(2) annealing the seeded layers at a temperature of at least about 550°C for a time of less than or equal to about 3 minutes.

44. (Original) The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration of at least 10^{20} atoms/cm^3.

45. (Original) The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^3 fold higher than any dopant concentration in the second silicon-containing layer.

46. (Original) The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^5 fold higher than any dopant concentration in the second silicon-containing layer.

47. (Original) The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^{10} fold higher than any dopant concentration in the second silicon-containing layer.

48. (Original) The method of claim 42 wherein the second silicon-containing layer is substantially undoped.

Claims 49-73 (Cancelled).

REMARKS

Claim 42 is amended. Claims 42-48 are pending in the application.

Claims 42-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Al-Shareef, U.S. Patent No. 6,111,285, in view of Thakur, U.S. Patent No. 6,255,159. The Examiner is reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Claims 42-48 are allowable over the cited combination of Al-Shareef and Thakur for at least the reason that the references, individually or as combined, fail to disclose or suggest each and every limitation in any of those claims.

As amended independent claim 42 recites forming a container construction having an exposed outer periphery defined by a first silicon-containing layer and an exposed inner periphery defined by a second silicon-containing layer. Claim 42 further recites the first silicon-containing layer being more heavily doped than the second silicon-containing layer. Additionally, claim 42 recites converting at least some of each of the first and second silicon-containing layers to hemispherical grain silicon (HSG) with the first silicon-containing layer having smaller average grain size HSG than the second silicon-containing layer, and forming a dielectric material along the exposed inner and outer peripheries of the container construction. The amendment to claim 42 is supported by the specification at, for example, Figs. 11-13 and the accompanying text at paragraphs 48-51.

Al-Shareef discloses forming a layer comprising HSG by depositing a layer of doped polysilicon followed by depositing a layer of undoped HSG (col. 4, ll. 1-11 and Fig. 6). Al-

Shareef does not disclose or suggest the claim 42 recited forming a container construction having an exposed outer periphery defined by a first silicon-containing layer and an exposed inner periphery defined by a second silicon-containing layer, the first silicon-containing layer being more heavily doped than the second silicon-containing layer. Nor does Al-Shareef disclose or suggest the recited converting at least some of each of the first and second silicon-containing layers to HSG. Further, Al-Shareef does not disclose or suggest the claim 42 recited first silicon-containing layer having smaller average grain size HSG than the second silicon-containing layer.

Thakur discloses a first container embodiment having pillars of doped silicon 106 surrounded by layers of undoped amorphous silicon 104 and 108 (col. 44, ll. 55-57 and Fig. 1F). The two amorphous undoped layers 104 and 108 are subsequently seeded and converted to HSG (col. 5, ll. 3-15 and Fig. 1H). Thakur discloses an alternative embodiment comprising a trench capacitor having an exposed undoped layer 408 within an opening (col. 6, ll. 63 through col. 7, ll. 20 and Figs. 4D and 4E). Thakur does not disclose or suggest the recited container construction having an exposed inner periphery defined by a second silicon-containing layer and an exposed outer periphery defined by a first silicon-containing layer which is more heavily doped with conductivity enhancing dopant than the second silicon-containing layer. Additionally, Thakur does not disclose or suggest the claim 42 recited converting at least some of each of the first and second silicon-containing layers to HSG where the more heavily doped first silicon-containing layer has smaller average grain size HSG than the second silicon-containing layer. As combined, Al-Shareef and Thakur fail to disclose or suggest the claim 42 recited forming a container construction having an exposed inner periphery defined by a second silicon-containing layer and an

exposed outer periphery defined by a first silicon-containing layer which is more heavily doped with conductivity enhancing dopant than the second silicon-containing layer, and converting at least some of the first and the second layers to hemispherical grain silicon, the first silicon-containing layer having a smaller average grain size HSG than the second silicon-containing layer. Accordingly, independent claim 42 is not rendered obvious by the cited combination of Al-Shareef and Thakur and is allowable over these references.

Dependent claims 43-48 are allowable over the cited combination of Al-Shareef and Thakur for at least the reason that they depend from allowable base claim 42.

For the reasons discussed above claims 42-48 are allowable. Accordingly, applicant respectfully requests formal allowance of pending claims 42-48 in the Examiner's next action.

Respectfully submitted,

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